Evaluating Methods of Improving Phase-Locked Loop Performance

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Abstract

This paper investigates methods to enhance the dynamic response of Phase-Locked Loops (PLLs), which are critical components in telecommunications and computing for signal synchronization. Focusing on lock time and transient behavior, two improvements are examined: the dual-loop design and the dual-edge triggered phase frequency detector (PFD). The dual-loop approach utilizes a wide-bandwidth loop for rapid acquisition and a narrow-bandwidth loop for precise tracking, while the dual-edge triggered PFD doubles feedback frequency by using both rising and falling edges of input signals. Experimental data demonstrates that both architectures significantly reduce initial overshoot and decrease lock time compared to the standard design, with the dual-edge triggered PFD achieving lock two cycles faster and the dual-loop design six cycles faster. Future investigations will include digital-based features, more thorough testing metrics, and novel enhancement techniques.

1. Introduction

1.1 What is a Phase-Locked Loop (PLL)?

A Phase-Locked Loop (PLL) is a feedback control system for the synchronization of a generated feedback signal with a reference signal. They are essential for frequency synthesis, clock recovery, and SERDES applications in telecommunications and computing [1]. This paper examines methods to improve a PLL's dynamic response, focusing on two architectures: the dual-loop design and the dual-edge triggered phase frequency detector.

2. Literature Review and Observations

The field of PLL design has seen continuous innovation aimed at improving performance metrics such as lock time, phase noise, and power consumption. Different strategies for improving these metrics usually involve targeting individual components of the phase-locked loop architecture [2][3]. Strategies for improvement have also expanded to include digital and software features [4][5]. To compare performances, the root mean square (RMS) of the jitter and system lock time were considered.

2.1 Phase Locked Loop Architecture

The basic PLL is a feedback system composed of a Phase Frequency Detector (PFD), a Loop Filter (LF), and a Voltage-Controlled Oscillator (VCO).

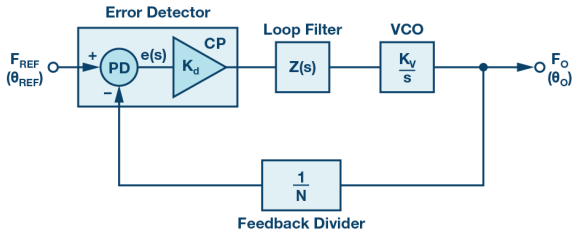


Figure 1: Basic PLL Architecture [1]

The PFD compares the phase and frequency of the reference signal with those of the feedback

signal from the VCO and drives a charge pump with "up" and "down" pulses whose widths are proportional to the phase difference. The pulses are smoothed by the LF and applied to the VCO, changing the frequency accordingly. This feedback loop works to bring the phase difference to zero, at which point the PLL is "locked".

2.2 Phase Locked Loop Dynamic Response

The dynamic response of a PLL is its transient behavior as it acquires lock [6]. Key metrics for evaluating dynamic response include lock time, overshoot, and ripple. Lock time is the time from when the PLL detects a change in the reference frequency to when the output frequency settles within a specified tolerance of the target frequency. There is no single method to determine the optimal lock time, since varying architectures respond differently to one definition of locking. Overshoot and ripple refer to the transient fluctuations in the output frequency or phase during acquisition.

2.2.1 Dual-Loop Architectures

A “dual-loop” architecture may be interpreted in many different ways. Common builds either include two or more PFD paths or feed the output of one PLL into another. Such designs are effective when jitter, phase noise, acquisition speed, or a large bandwidth are the main metrics to be considered, particularly when multiple metrics are of concern [7][8][9].

The dual-loop architecture addressed in this paper is the cascading type. It targets the trade-off between fast acquisition and stable tracking by employing two separate loops: a wide-bandwidth loop for fast initial frequency acquisition, and a narrow-bandwidth loop for fine phase tracking [10].

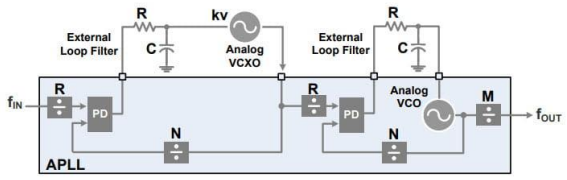


Figure 2: Skyworks’ Dual-Loop Architecture [10]

2.2.2 Dual-Edge Triggered Phase Frequency Detector Architectures

A standard PFD uses only the rising edges of its input signals to detect phase differences. A dual-edge triggered PFD, however, utilizes both the rising and falling edges of the reference and feedback signals.

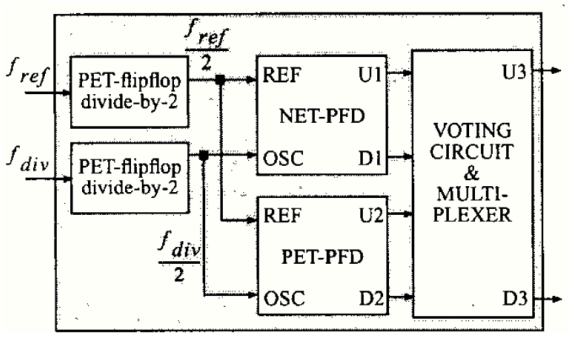


Figure 3: Dual-Edge Triggered PFD [11]

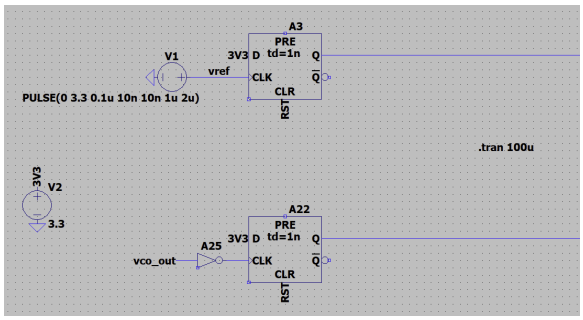
By doubling the number of phase-error instances per cycle, the dual-edge triggered PFD provides more frequent feedback to the loop filter, allowing the PLL to respond more quickly to phase and frequency changes [12].

3. Procedure

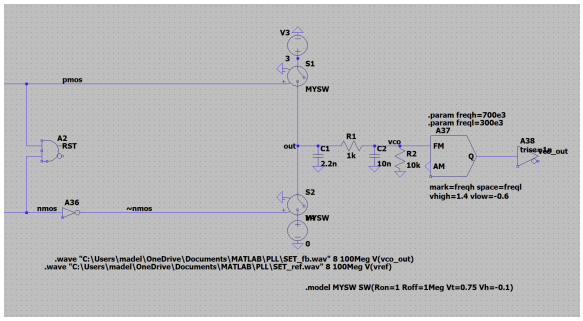
To examine these architectures and their effects on PLL performance, I created a simulatable model in LTspice and analyzed the data with MATLAB.

3.1 Simulation

The phase detector part of the model is shown in Figure 4a and consists of two D flip-flops. Figure 4b shows the charge pump, which is built with two voltage-controlled switches and a filter leading to the VCO.



(a)



(b)

Figure 4 (a) first half of the PLL model and (b) second half of the PLL model.

Building the model consumed more time than anticipated for the following reasons:

1. LTspice simulates switching slowly:

LTspice's weakness is simulating fast switching. As the model grew in complexity, so did the simulation time. This meant that the method of modeling the switching components, such as the phase-frequency detector and charge pump, had to be as simple as possible, while not compromising detail.

2. The desired model level:

To be able to explore the PLL architecture with adequate detail, a model must be at a low enough level to access these details. However, more detail in a model sacrifices simulation time.

Regardless of these constraints, the constructed model allowed me to adjust the parameters of interest while simulating quickly.

3.2 Data Analysis

To analyze the simulation data, the graph data was downloaded into a WAV file format and imported into MATLAB. I wrote MATLAB code to calculate and plot the jitter time for each variation of the phase locked loop.

3.3 Data plots

The following data shows clear improvement with both architectures mentioned above. The plots include two lines that mark a 50% and 10% error in the feedback signal from the reference signal. A system is defined as "locked" when it has reached three consecutive cycles with less than 10% error.

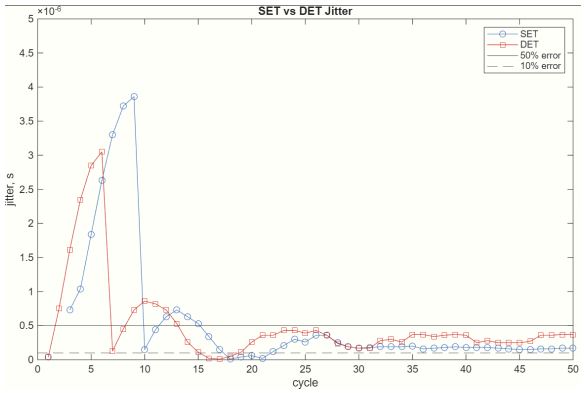


Figure 5: Data plot showing the dynamic responses of PLLs with a single-edge triggered PFD (blue) and dual-edge triggered PFD (red)

The initial overshoot for the dual-edge triggered PFD system is significantly decreased compared

to the single-edge triggered system, and it acquires two cycles faster.

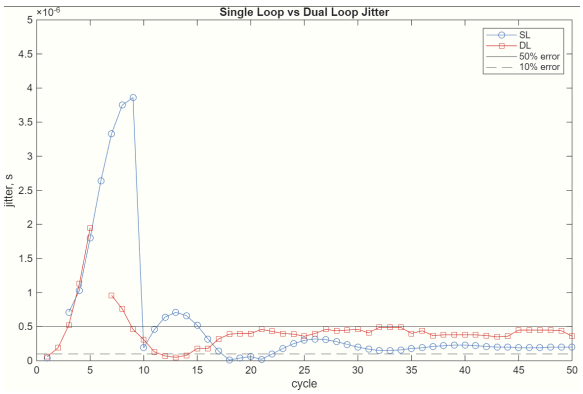


Figure 6: Data plot showing the dynamic responses of a single-loop PLL (blue) and dual-loop PLL (red)

The initial overshoot for the dual-loop system is also significantly decreased, and it acquires six cycles faster than the single-loop architecture.

4. Conclusion

The data demonstrated that both the dual-loop and dual-edge triggered PFD architectures significantly enhance PLL dynamic response, with the dual-edge triggered PFD increasing lock time by two cycles, while the dual-loop design achieved a six-cycle faster lock. These findings demonstrate the efficacy of focusing on the dynamic response of a PLL for improving its performance.

4.2.1 Simulating Digital Logic-Dependent Features

Future work will extend the current simulation to incorporate digital logic-dependent features. This includes simulating a lock detect circuit to indicate when the PLL has achieved and maintained lock. Additionally, future research will implement an error-based feedback mechanism to dynamically adjust loop parameters, such as the loop filter bandwidth, optimizing performance in real time.

4.2.2 Advanced Performance Evaluation

To provide a more comprehensive analysis, future research will incorporate more advanced performance evaluation methods, such as clearer jitter and lock time analyses for a larger variety of use cases. Additionally, the phase noise of each architecture will be analyzed. These metrics are essential for assessing the overall quality and stability of the output signal.

4.2.3 New Theories for Performance Enhancement

Future work will explore novel theoretical approaches that target deeper areas of PLL architecture to enhance performance. The goal is to move beyond conventional PLL architectures and discover new models for achieving faster and more robust designs.

5. References (need to be properly formatted)

[1] I. Collins, “Phase-locked loop (PLL) fundamentals,” Phase-Locked Loop (PLL) Fundamentals | Analog Devices, https://www.analog.com/en/resources/analog-dialogue/articles/phase-locked-loop-pll-fundamentals.html.

[2] X. Xu, W. Rhee and Z. Wang, "Enhanced FIR-embedded noise reduction method with hybrid phase detection for semidigital fractional-N phase-locked loops," 2019 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Chengdu, China, 2019, pp. 94-95

[3] C. -W. Hsu, K. Tripurari, S. -A. Yu and P. R. Kinget, "A Sub-Sampling-Assisted Phase-Frequency Detector for Low-Noise PLLs With Robust Operation Under Supply Interference," in IEEE Transactions on Circuits

and Systems I: Regular Papers, vol. 62, no. 1, pp. 90-99, Jan. 2015

[4] A. Godave, P. Choudhari and A. Jadhav, "Comparison and Simulation of Analog and Digital Phase Locked Loop," 2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), Bengaluru, India, 2018, pp. 1-4

[5] H. Sefraoui, K. Salmi, H. Chadli and A. Ziyyat, "Adaptive Locking Range of the Software Phase-Locked Loop (SPLL)," 2022 International Conference on Electrical, Computer and Energy Technologies (ICECET), Prague, Czech Republic, 2022, pp. 1-5

[6] [1] S. Long, “Phase Locked Loop Circuits,” in *Prof. Steve Long,* https://web.ece.ucsb.edu/~long/ece594a/PLL_intro_594a_s05.pdf

[7]V. Manthena, S. Miryala, G. Deptuch and G. Carini, "A 1.2-V 6-GHz Dual-Path Charge-Pump PLL Frequency Synthesizer for Quantum Control and Readout in CMOS 65-nm Process," 2020 11th IEEE Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON), New York, NY, USA, 2020, pp. 0570-0576

[8] Z. Yang, Y. Chen, S. Yang, P. -I. Mak and R. P. Martins, "A 10.6-mW 26.4-GHz Dual-Loop Type-II Phase-Locked Loop Using Dynamic Frequency Detector and Phase Detector," in IEEE Access, vol. 8, pp. 2222-2232, 2020

[9] Loke, Alvin & Barnes, Robert & Wee, Tin Tin & Oshima, Michael & Moore, Charles & Kennedy, Ronald & Gilsdorf, Michael. (2006). A versatile 90-nm CMOS charge-pump PLL for SerDes transmitter clocking. Solid-State Circuits, IEEE Journal of. 41. 1894 - 1907.

[10] [1] “Optimizing Clock Synthesis in Small Cells and Heterogeneous Networks.” Skyworks Inc, Irvine, CA, https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/white-papers/Optimizing-Clock-Synthesis-in-Small-Cells-and-Heterogeneous-Networks.pdf

[11] S. I. Ahmed and R. D. Mason, "A dual edge-triggered phase-frequency detector architecture [frequency synthesizer applications]," Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03., Bangkok, Thailand, 2003, pp. I-I

[12] Kyung Ho Ryu, Sang Kyu Park, and Seong-Ook Jung. 2008. A dual-edge triggered phase detector for fast-lock DLL. In Proceedings of the 12th WSEAS international conference on Circuits (ICC'08). World Scientific and Engineering Academy and Society (WSEAS), Stevens Point, Wisconsin, USA, 197–201.